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Optimized Resonant Pulsed Power Supplies with Deadbeat - Repetitive Regulation

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***Abstract*—This paper presents a novel digital deadbeat + repetitive control (DBRC) strategy for output voltage regulation of pulsed power resonant converters used in high energy physics applications. The proposed converter contains three individual series resonant parallel loaded (SRPL) converter arms, which effectively mitigate the influence of resonant tank unbalances on the converter operation. The deadbeat controller is designed to produce fast dynamics of the voltage pulses during the system transient periods, while the repetitive controller is employed to counteract model uncertainties and component variations and hence to achieve a high performance and fine quality in the steady state.**

Keywords—resonant converters; deadbeat control; repetitive control; pulsed power; soft switching

I. INTRODUCTION

Long pulse power modulators used for high energy particle acceleration experiments are required to generate a series of high power, high voltage pulses in order to drive klystron tubes, each pulse lasting typically a few milliseconds in length. As the most important criterion, the pulse magnitude needs to be stable and predictable so that any variation in it has a limited and acceptable influence on the acceleration. Traditional power supplies used for accelerating the particles are based upon line frequency technology that demands bulky transformers and passive components [1]. The increasingly more demanding specifications on the pulse voltage quality cannot be met by the current technology while maintaining acceptable cost and size limits.

Over the last two decades, motivated by advances in semiconductor devices and high speed microcontrollers, power electronics based, high frequency resonant converters have attracted more and more research interest. Compared with conventional power supplies, the high frequency operation mode ensures compact size and light weight of passive components, while the use of resonant circuits arranges the voltage/current to be zero at switching instant to achieve high efficiency conversion [2]. Many works have been reported in literature to demonstrate the concept of pulsed power resonant power converters used for the high energy physics applications.

A three-phase series resonant parallel loaded (SRPL) resonant converter solution was first discussed in [3]. To assess the semiconductor losses and reliability under thermal cycle stress, a single phase variant was also considered in [4], and only an open loop control was utilized for the output voltage regulation. Based on the DQ modeling approach, a multi-variable state feedback controller was presented in [5], in order to overcome limitations of the open loop control method. However, the performance of the three-phase topology is quite sensitive to component physical discrepancy such as resonant tank unbalances. This also compromises the voltage ripple quality and downgrades the multi-variable state controller performance.

Taking the aforementioned limitations into account, reference [6] demonstrated a three-single phase SRPL converter topology and a PI + repetitive combined control (PIRC) strategy. The separate voltage scaling and rectification stage decoupled the influence of resonant tank unbalances on the converter operation effectively, while the learning nature of the repetitive controller improved the pulse voltage dynamics cycle by cycle, and eventually pushed the rise time towards the physical limitation of the converter with negligible overshoot. In spite of the high dynamic and steady state performance, this control solution demands a relatively long learning period, i.e. ten to twenty learning cycles, due to the design compromise of the PI controller used [6]. For the target applications, this implies a considerable waste of the energy, as the pulses generated during the learning transient of the repetitive controller are not qualified for the experiments.

This paper focuses on an intensive study on the voltage control of the pulsed power resonant converter proposed in [6]. A novel deadbeat + repetitive control (DBRC) strategy is proposed to improve the pulse voltage regulation. The deadbeat controller is designed to produce fast dynamics of the voltage pulses during the system transient period, while the plug-in type repetitive controller is employed to counteract model uncertainties and component variations and hence to achieve a high performance in the steady state. Combined frequency and phase shift modulation is applied to obtain soft-switching of semiconductor devices for high efficiency conversion.

II. CONVERTER STRUCTURE AND MODULATION

A. Topology

Figure 1 presents the structure of the three-single phase SRPL pulse power resonant converter. An active three-phase PWM rectifier is utilized to charge a DC-link capacitor bank. Three H-bridge inverters are implemented to produce three high frequency square-wave voltages (V_{TA}, V_{TB}, and V_{TC}) with phase shift of 120°. The SRPL tank configuration and high frequency transformer are employed in each phase to boost the voltage to the level that is required by the load. Three single phase rectifiers plus LC filters are adopted to

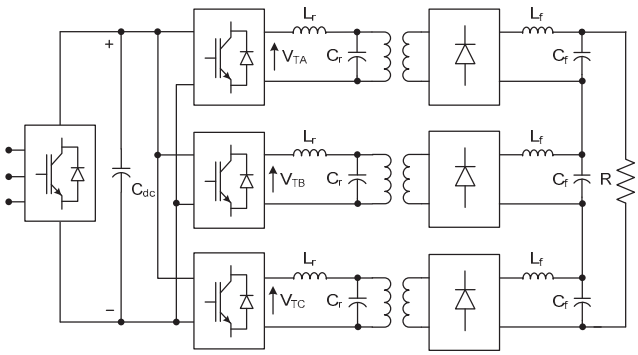


Figure 1 Three-single phase SRSL resonant power converter structure.

attain a low ripple output voltage and the filter capacitors are connected in series to supply the load.

For each phase, the output scaling and rectifying stage i.e. including the transformer, rectifier, filter, and equivalent DC load resistance, can be modeled as an equivalent AC resistor R_{AC} as expressed in (1), where N_T is the transformer turns ratio. For a given tank quality factor Q and resonant frequency ω_r, the resonant inductor and capacitor can be derived as in (2) and (3), respectively.

$$R_{AC} = \frac{N_T{}^2 \pi^2 R}{24} \tag{1}$$

$$L_r = \frac{R_{AC}}{Q\omega_r} \tag{2}$$

$$C_r = \frac{Q}{R_{AC}\omega_r} \tag{3}$$

B. Operation

The PWM rectifier is only enabled to charge the DC-link capacitor between two pulses. Since it can be operated with unity displacement power factor and high quality current, the influence on the utility supply can be significantly minimized compared to the traditional approaches [1].

During each pulse generation, the DC-link capacitor provides all the energy. A large drop level, e.g. generally 15%-30%, is allowed on the capacitor voltage level. This indicates a significant volume reduction of the capacitor bank and the whole conversion system. A mutual phase shift of 120º has been set among the three square-wave voltages to achieve ripple cancellation on the load side. The SRPL resonant tank topology has been selected since it is particularly suitable for high voltage long pulse applications [3]. During the converter modulation, both the frequency and phase shift are adjusted, in order to maintain the pulse voltage constant and achieve soft switching of semiconductor devices, along with the continuous drop of the DC-link voltage.

C. Modulation

It has been demonstrated in [3] that, using frequency modulation or phase shift modulation alone is not possible to maintain the soft switching of semiconductor devices throughout the whole pulse period. For the power levels at which such converters will be used, devices hard switching leads to a steep increment on the switching losses, and thus makes the proposed solution technically unfeasible for the target applications. The combined frequency and phase shift modulation approach is then selected to control the H-bridge inverters to ensure soft switching.

Assuming the H-bridge inverter is switched close to the tank resonant frequency and the tank is reasonably selective (i.e. Q≥2.0), only the fundamental component of the square wave voltages is considered to drive the SRSL tank. The phase shift ψ between the fundamental input tank voltage and current can be derived by analyzing the equivalent LCR circuit formed by resonant inductor, capacitor and AC resistor (R_{AC}), as expressed in (4), where F is the ratio between the switching frequency and the tank resonant frequency. An modulation index *MI*, for a phase and frequency regulated resonant converter with zero current switching, is given in (5). Detailed switching pattern and transition analysis can be found in [3, 6].

$$\psi = arctan(QF^3 + \frac{F}{Q} - FQ) \tag{4}$$

$$MI(F) = \frac{Q}{(F^4Q^2 + F^2 - 2F^2Q^2 + Q^2)\sqrt{F^2Q^2 + 1}} \tag{5}$$

III. DQ Modeling

The modeling process for resonant converters needs to take into account high frequency state variables introduced by the resonant stage. Reference [5] has demonstrated that the DQ modeling technique can represent the resonant converter dynamics and steady state behavior accurately. In this work, the DQ modelling has also been adopted to analyze the converter.

Considering that the PWM rectifier is modulated to charge the DC-link capacitor only when the output voltage pulse is null, it can be excluded from the modeling and control design point of view. Assuming that ideal electrical elements are implemented, unbalances among the resonant tanks and leakage inductances of the high-frequency transformers can be neglected. Figure 2 shows a DQ circuit model for the proposed resonant converter, where V_d is the peak amplitude of the fundamental component of the tank input voltage; ω is the converter operating frequency; K and V_{out} are defined in (6) and (7), respectively. Detailed modelling procedure and the state space description can be found in [6].

$$K = \frac{N_T{}^2 \pi^2}{24} \tag{6}$$

$$V_{out} = \frac{6\sqrt{E_d{}^2 + E_q{}^2}}{N_T \pi} \tag{7}$$

Figure 3 shows an open loop test of the converter circuit and developed DQ model. The perfect match in the dynamic

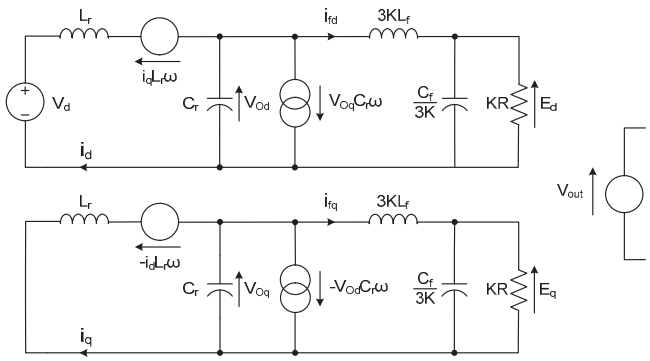


Figure 2 Equivalent DQ circuit model.

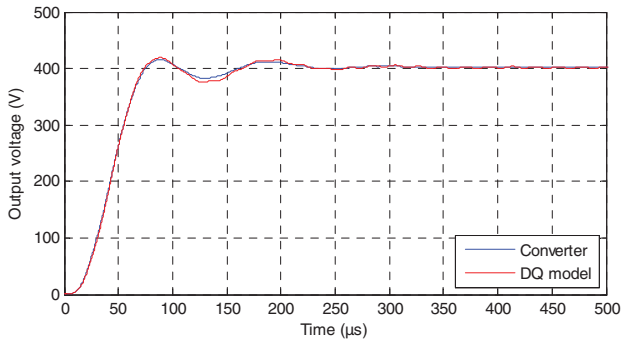


Figure 3 Open loop test of the converter circuit and developed DQ model.

responses of the two models confirms the modeling accuracy.

IV. Control Strategy

For this application, four requirements are imposed to the output pulse voltage regulation: first, the pulse rise time should be less than 100μs; second, the overshoot of the pulse voltage should not exceed 3%; third, the demand pulse amplitude needs to be maintained throughout the whole pulse duration; fourth, qualified voltage pulses should be available as soon as the converter system enables.

Taking all the requirements into account, a novel DBRC strategy is proposed, in order to achieve both a fast transient regulation and high performance in steady state. Figure 4 shows a generalized control block diagram, where *R(z)*, *RC*, *DB*, $G_p(z)$, *D(z)* and *Y(z)* represent the pulse voltage reference, repetitive controller, deadbeat controller, system plant, lumped disturbance signal, and converter pulse voltage output, respectively.

A. Deadbeat Control Design

Owing to its high control bandwidth feature, deadbeat control has been considered widely for digital control implementations demanding fast dynamic response. For linear time-invariant (LTI) systems, it is capable of determining an actuating signal to bring the controlled variable to the steady state in the smallest number of sampling time steps. The main drawback of the deadbeat controller is the high sensitivity to model uncertainties, parameter mismatches, and measurement noises. Since it is based on pole-zero cancellation, a good knowledge of the target plant is required. Otherwise, the control performance is strongly reduced in presence of unpredicted disturbances such as dead times, as there is no inherent integral action involved [7].

Considering the load resistance reasonably constant throughout the pulse generation and one unit delay representing hardware sampling and modulation time, the system plant can be expanded and analyzed in the discretized domain at sampling frequency of 40kHz, and the corresponding pole-zero map can be evaluated as shown in Figure 5.

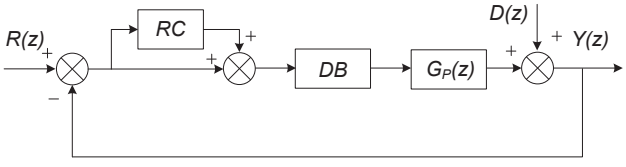


Figure 4 Proposed DBRC block scheme.

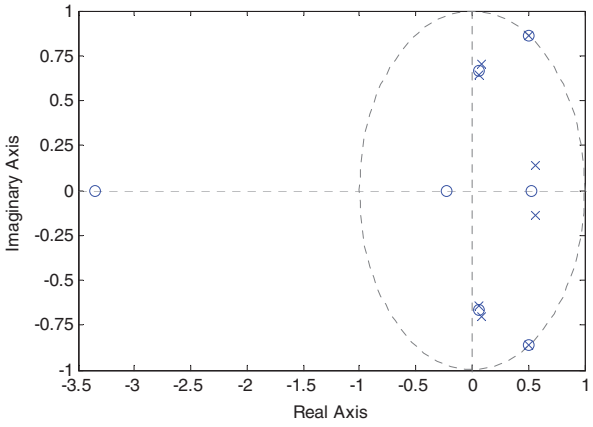


Figure 5 Pole-zero map of the system plant.

Clearly, two pole pairs of 0.51±0.86i are completely cancelled by associated zero pairs. Thereby, their influence can be neglected during the control design procedure. By considering only the remaining poles and zeros, a simplified system plant can be obtained. As shown in Figure 6, the step response of the simplified plant is very close to that of the original system.

For the deadbeat control design, the simplified plant transfer function is applied, due to the following considerations: first, it leads to a simple deadbeat controller structure for easy hardware implementation; second, the relatively straightforward deadbeat control loop relieves the complexity of the following repetitive control design; third, it avoids introducing the high frequency poles and zeros of the deadbeat controller, which makes the whole control system less sensitive to model uncertainties such as components discrepancy, noises and switching dead time. The complete deadbeat controller is expressed as in (8).

$$G_{DB}(z)=\frac{z^5-1.3z^4+z^3-0.62z^2+0.167z}{2z^5-0.62z^4-0.7z^3-1.4z^2+0.53z+0.184} \quad (8)$$

B. Repetitive Control Desigm

Repetitive control is attracting more and more research interest in modern industrial applications for feedback systems that are subject to periodic reference inputs or periodic disturbances. Based on the internal model principle [8], the repetitive controller processes the error signal calculated with the same sample of the previous waveform period and applies the resultant signal to improve the control performance of the current cycle. Theoretically, with a suitably designed repetitive controller, the output of a stable feedback system can track the periodic reference signal or/and reject the exogenous periodic disturbance with zero

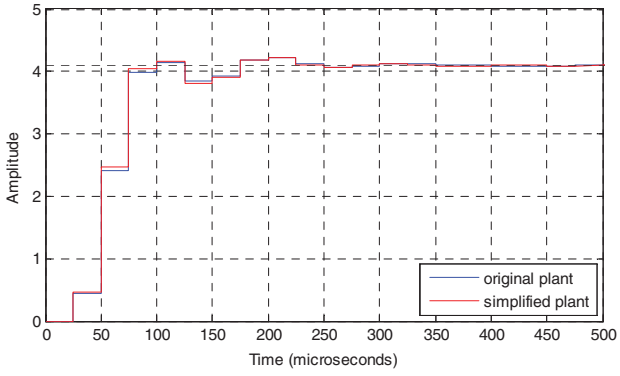


Figure 6 Step response comparison of original plant and simplified plant.

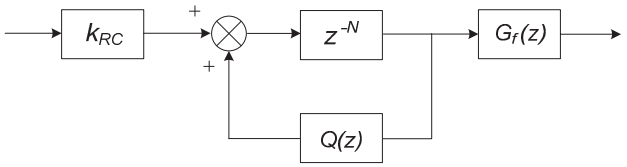


Figure 7 Detailed structure of the plug-in RC.

steady state error even in the presence of model uncertainties.

In this work, a plug-in type RC is designed to achieve excellent steady state performance of the pulse voltage regulation. Figure 7 shows the detailed controller structure, where k_{RC} is the repetitive learning gain, z^{-N} is the delay line, N is the ratio between the time period of the reference signal and the digital sampling time, $Q(z)$ is the robustness filter, and $G_f(z)$ is the stability filter.

The use of the robustness filter $Q(z)$ is to modify the internal model and thus to effectively increase the system stability margin. A constant of 0.9 has been chosen in this work, due to its simple implementation. The stability filter $G_f(z)$ is employed to ensure that the overall control system is stable after the introduction of RC. The design of $G_f(z)$ is coupled with the value of k_{RC}, and is also correlated with the selection of $Q(z)$. It is often designed as the inverse of the closed loop transfer function for minimum phase systems or a zero phase error tracking compensator for non-minimum phase ones [9, 10]

According to the small gain theorem [11], two sufficient stability conditions for the plug-in RC system can be summarized as follows: (a) the original control system, i.e. without the plug-in type RC, is inherently stable; (b) equation (9) is guaranteed for all the frequencies below the Nyquist frequency ω_{nyq}, where T_s is the sampling time of the digital control system.

$$\left| Q(e^{j\omega T_S}) - \frac{k_{RC}\, G_f(e^{j\omega T_S}) G_{DB}(e^{j\omega T_S}) G_P(e^{j\omega T_S})}{1 + G_{DB}(e^{j\omega T_S}) G_P(e^{j\omega T_S})} \right| < 1 \quad (9)$$

The first condition can be guaranteed, as the deadbeat controller has been properly designed. A time advance unit of z^4 has been selected here as a simple structure for $G_f(z)$. With the robustness filter $Q(z)$ of 0.9, the range of the repetitive gain k_{RC} can be evaluated accordingly by examining the Nquist locus curve of equation (9). As shown in Figure 8, the locus curve, with k_{RC} of 0.4, stays within in the unitary circle for the entire frequency range up to ω_{nyq}. This implies that the second condition is satisfied, and thus the overall control system is adequately stable. Table I summarizes the design result of the plug in RC.

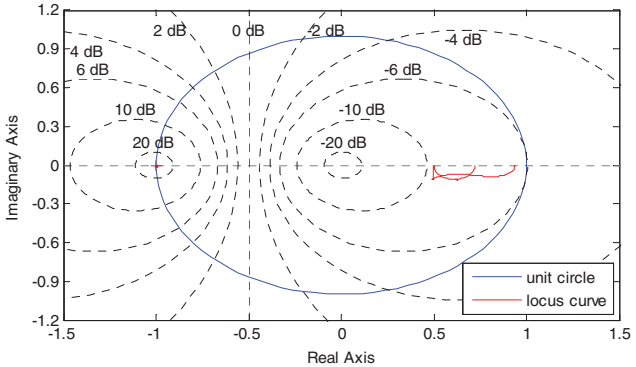


Figure 8 Nyquist locus curve of equation (9) with $G_f(z)$ of z^4, k_{RC} of 0.4 and $Q(z)$ of 0.9.

TABLE I. REPETITIVE CONTROLLER PARAMETERS

Symbol	*Description*	*Value*
f_S	Sampling frequency	40kHz
N	Delay chain	40
k_{RC}	Repetitive gain	0.4
$Q(z)$	Robustness filter	0.9
$Gf(z)$	Stability filter	z^4

TABLE II. PROTOTYPE CONVERTER PARAMETERS

Symbol	*Description*	*Value*
V_{out}	Pulse voltage amplitude	375V
P_{out}	Pulse peak power	3kW
V_{DC}	Initial DC-link voltage	110V
ΔV_{DC}	DC-link droop level	25%
Q	Tank quality factor	2.5
L_r	Resonant inductance filter	53.2μH
C_r	Resonant capacitance	1μF
N_T	Transformer turns ratio	1:1
L_f	Filter inductance	0.3mH
C_f	Filter capacitance	1.2μF

V. SIMULATION AND EXPERIMENTAL RESULTS

With the aim of verifying the proposed DB+RC control concept, experimental results obtained from a reduced scale prototype converter rated at 3kW are presented and compared with simulation. Figure 9 presents a photograph of the prototype converter, while Table II summarizes the converter circuit parameters. A DSP/FPGA based digital control platform has been utilized for control code implementation.

Figure 10 shows the first pulse voltage generated by the prototype converter, where only the deadbeat controller takes action. Compared to the result presented in [6], the proposed deadbeat controller can offer a very fast dynamic response. The rise time of the first pulse voltage is approximately 70μs, value which is acceptable for the application requirements. The pulse amplitude keeps constant through 1ms pulse period and the peak-to-peak voltage ripple is less than 1%, though a slight undershoot can be observed.

The plug-in RC starts to work from the second pulse generation, and reaches its steady state quickly at the fifth pulse. As shown in Figure 11, the undershoot occurred at the first pulse can be eliminated, resulting a perfect voltage

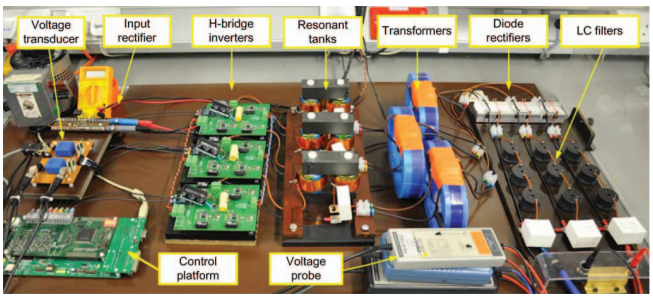
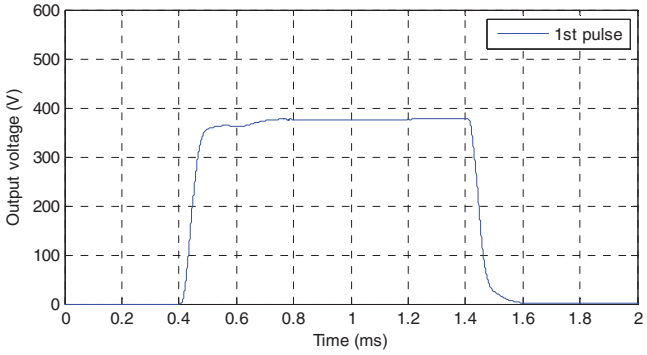
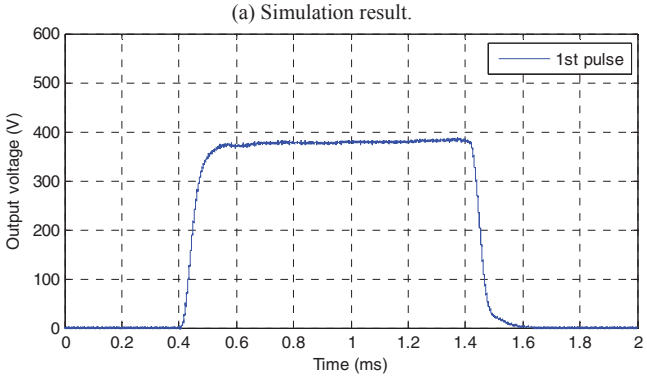


Figure 9 Experimental prototype converter.

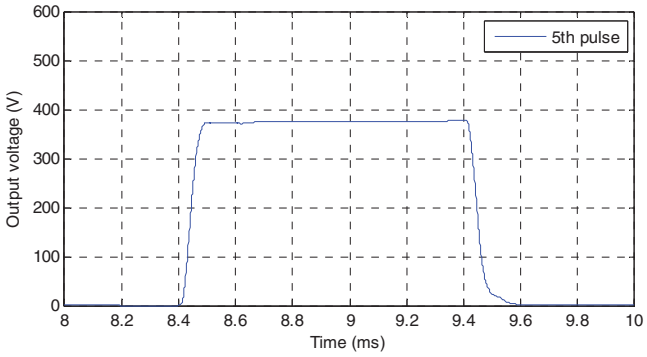


(a) Simulation result.

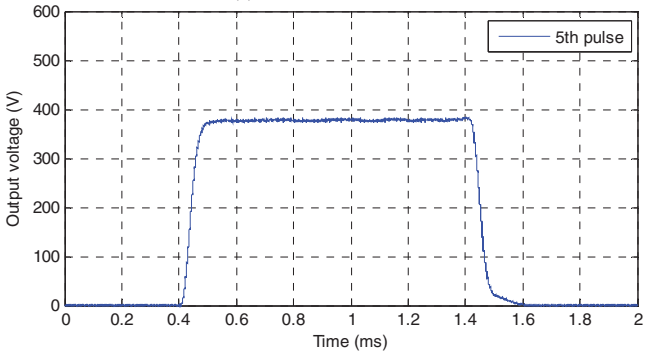


(b) Experimental result.

Figure 12 First voltage pulse, with DB control only.

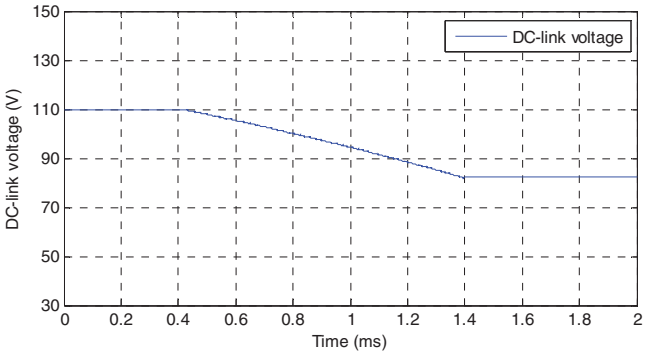


(a) Simulation result.

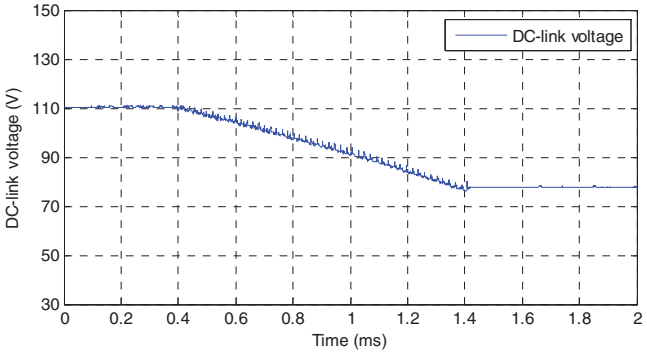


(b) Experimental result.

Figure 13 Fifth voltage pulse, with DB+RC control.

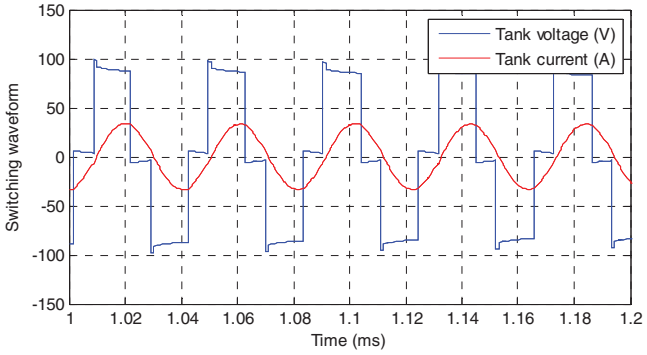


(a) Simulation result.

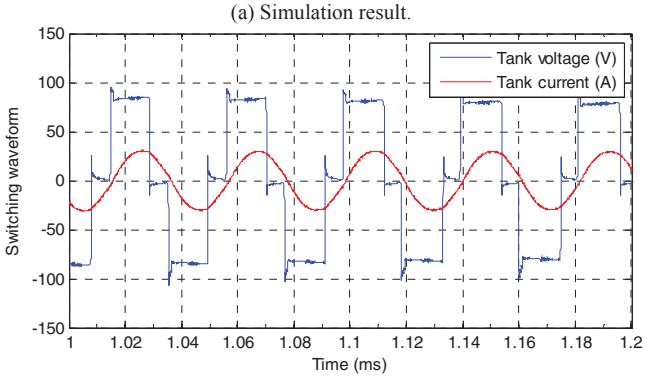


(b) Experimental result.

Figure 10 DC-link voltage throughout pulse generation.



(a) Simulation result.



(b) Experimental result.

Figure 11 Switching waveform of Phase C.

pulse with rise time of 50μs, value which is close to the physical limitation of the converter. In compassion of the PI+RC control solution demonstrated in [6], the proposed DB+RC strategy is capable of producing a fast pulse dynamic and reaching the RC steady state within four learning cycles only. For the target applications, this implies a considerable improvement of the system boost time and a significant energy saving during the RC learning transient.

Figure 12 presents the DC-link voltage during the pulse voltage generation. A large voltage drop of 27%, i.e. from 110V to 80V, is allowed, while the combined frequency and phase shift modulation is still capable of maintaining constant voltage amplitude.

Figure 13 highlights the switching waveform of the H-bridge inverter Phase C. The IGBTs in the lagging leg are always switched at the zero crossing point of the tank current, while the ones in the leading pair have soft switching on and hard switching off. Snubber capacitors can be utilized to achieve zero voltage switching off [4]. Consequently, soft-switching can be obtained at full power

in all the IGBTs, which leading to a highly efficient energy conversion.

VI. Conclusions

This paper proposed a novel deadbeat + repetitive control solution for the output voltage regulation of pulsed power resonant converters used in high energy physics applications. In compassion of previous control techniques, it is capable of producing a fast pulse dynamic and reaching the RC steady state quickly in four learning cycles. For the target applications, this implies a considerable improvement of the system boost time and a significant energy saving during the RC learning transient. Simulation and experimental results demonstrate the feasibility of the proposed control concept.

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